Abstracts

3.4 V operation 1 W MMIC power amplifier with SrTiO/sub 3/ capacitors for digital cellular phones

K. Yamaguchi, T.B. Nishimura, N. Iwata, K. Takemura, M. Kuzuhara and Y. Miyasaka. "3.4 V operation 1 W MMIC power amplifier with SrTiO/sub 3/ capacitors for digital cellular phones." 1997 MTT-S International Microwave Symposium Digest 3. (1997 Vol. III [MWSYM]): 1403-1406.

This paper describes 950 MHz power performance of a two-stage MMIC amplifier utilizing n-AlGaAs/InGaAs/n-AlGaAs FETs and SiTiO/sub 3/ capacitors. Under 3.4 V drain bias operation, the MMIC with 2.0/spl times/2.4 mm/sup 2/ area delivered a /spl pi//4-shifted QPSK output signal of 0.8 W (29.0 dBm), a power-added efficiency (PAE) of 30% and an associated gain of 26.4 dB with an adjacent channel leakage power at 50 kHz off-center frequency of -50.5 dBc. It also achieved a saturated output power of 1.1 W with PAE of 39%.

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